whereby polishing the insulator produces a floating gate and insulator layer, see figs. 1A-14E, cols. 1-14.

Applicants respectfully traverse the Examiner's rejection. As amended, Claims 1 and 7 each recite:

> depositing a dielectric layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

Depositing the dielectric layer on the planar surface facilitates lithographical patterning and etching of polysilicon control gate at a subsequent step. In contrast, the above-quoted limitations are neither disclosed nor suggested in Yamauchi. Instead, Yamauchi teaches deposition of a polysilicon layer 15 (See Yamaguchi's Figs. 13 and 14D, col. 10, lines 37-44). As a result, Yamauchi's dielectric layer 9 is deposited on an uneven surface, thus not achieving the benefits that Applicants' Claims 1 and 7 achieved. Accordingly Claims 1-2, 4-8 and 10-12 are allowable over Yamauchi.

The Examiner rejected Claims 1-2, 4-8, and 10-12 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,051,467 ("Chan"). The Examiner states:

> Chan et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 10; forming tunnel oxide 16 on the substrate; depositing a floating gate layer 18 on the tunnel oxide, the floating gate layer having a first thickness; etching the floating gate layer to form floating gate 18; depositing an insulator 30 on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and polishing the insulator until the second thickness is substantially equal to the first thickness (fig. 5), whereby polishing the insulator produces a floating gate and insulator layer, figs. 11, cols. 1-8.

Applicants respectfully traverse the Examiner's rejection. Chan neither teaches nor suggests Applicants' Claims 1 and 7, which each recite:

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depositing a dielectric layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

The benefits of depositing the dielectric layer on a planar surface is discussed above, with respect to Yamaguchi. Like Yamaguchi, Chan discloses depositing a polysilicon layer 32 over the floating gate (See Chan's Figs, 6-11, and at col. 3, lines 28-37). Chan teaches that polysilicon layer 32 is a "key" feature that provides a desirable grain size, avoids implantation damage (Chan, at col. 3, lines 38-45), and provides an avenue for varying the width of control gate (Chan, at col. 4, lines 6-9). Thus, Chan teaches away from Claims 1 and 7 because, to modify Chan in the direction of Applicants' Claims 1 and 7 (i.e., to omit depositing polysilicon layer 32 in favor of depositing the dielectric layer on the planar surface), would destroy the utility of Chan's disclosed device. Accordingly, Applicants respectfully submit Applicants' Claims 1-2, 4-8 and 10-12 are allowable over Chan.

The Examiner rejected Claims 1-2, 5, 7-8 and 11 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,033,956 ("Wu"). The Examiner states:

> Wu discloses a method for forming a semiconductor device, which comprises providing a substrate 200; forming tunnel oxide 202 on the substrate; depositing a floating gate layer on the tunnel oxide, the floating gate layer having a first thickness; etching the floating gate layer to form floating gate 204; depositing an insulator 210 on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and polishing/planarizing the insulator until the second thickness is substantially equal to the first thickness, whereby polishing the insulator produces a floating gate and insulator layer, see figs. 1-4G, cols. 1-6.

Applicants respectfully traverse the Examiner's rejection. Claims 1 and 7 each recite:

> polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer;

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Contrary to the Examiner's assertion, Wu neither discloses nor suggests such polishing. Instead, Wu discloses a planarizing plasma etch (Wu's Fig. 2C, col. 1, lines 52-58) and a liquid-phase depositing technique (Wu's Fig. 4C, and col. 3, lines 10-14) to provide the insulator layer. Further, Wu teaches away from "depositing a dielectric layer on the planar surface over the exposed top surface of the floating gate and the insulator layer," as recited in Claims 1 and 7 by teaching forming "a thin oxide layer 412 ...on the upper surface of the polysilicon 404 using ... chemical vapor deposition." (Wu's Fig. 4D, and col. 3, lines 14-17). Thus, Applicants respectfully submit that Claims 1-2, 5, 7-8 and 11 are each allowable over Wu.

The Examiner rejected Claims 1-2, 4-8, and 10-12 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,808,339 ("Yamagishi"). The Examiner states:

> Yamagishi et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 11; forming tunnel oxide 51 on the substrate; depositing a floating gate layer on the tunnel oxide, the floating gate layer having a first thickness; etching the floating gate layer to form floating gate 52/53; depositing an insulator 54 on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and polishing the insulator until the second thickness is substantially equal to the first thickness, whereby polishing the insulator produces a floating gate and insulator layer, see figs. 1-12B, cols. 1-16.

Applicants respectfully traverse the Examiner's rejection. Claims 1 and 7 recite "forming an oxide on exposed surfaces of the floating gate." As explained in Applicants' Specification, at page 4, lines 15-18, such oxide prevents charge leakage from the floating gate. Yamagishi neither discloses nor suggests such oxide formation or its attendant benefits. Accordingly, Applicants respectfully submit that Claims 1-2, 4-8 and 10-12 are allowable over Yamagishi.

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The Examiner rejected Claims 3, 9, and 13-15 under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi, Chan, Wu, or Yamagishi taken with U.S. Patent 5,672,892 ("Ogura") or U.S. Patent 5,478,767 ("Hong") in view of Applicant' s admitted prior art. The Examiner states:

> However, the above references do not explicitly show using doped polysilicon or doped amorphous silicon for the floating gate, and thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate.
>
> It is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, Applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2. It is also well known in the art to thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate such will provide isolation (eliminate short circuit) from the adjacent gates or device elements, and keep charges within the floating gate. For example, Ogura et al. teaches thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate, see frgs. 1-5, cols. 1-16; Hong also teaches thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate, see figs. 1-4K, cols. 1-10.
>
> With respect to claims 3 and 9, the thickness of the layers are considered to involve routine optimization which has been held to the within the level of ordinary skill in art. Although the above references do not fall into the ranges of the inventor's disclosure, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to vary the thickness of the layers for optimization purposes. More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.
>
> Furthermore, the implanting energy, dosage, thickness, width are considered to involve routine optimization which has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as energy, dosage, thickness, width and temperature, etc. would have been obvious:
>
> * * *

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> Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any energy, concentration, thickness, width range suitable to the method in process of Yamauchi et al., U.S./5,962,889 or Chan et al., U.S./6,05 1,467 or Wu, U.S./6,033,956 or Yamagishi et al., U.S./5,808,339 in order to optimize the process.
>
> Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modifl the standard process of Yamauchi et al. or Chan et al. or Wu or Yamagishi et al. with the teaching of (Ogura et al. or Hong) and Applicant's admitted prior art because of the desirability to improve device reliability and performance ofthe device.

Applicants respectfully traverse the Examiner's rejection. The deficiencies in Yamaguchi, Chan, Wu and Yamagishi are already discussed above with respect to Claims 1 and 7. In addition, Ogura's oxide layer 26 is provided for a higher breakdown voltage (Ogura's col. 5, lines 17-26), and Hong's oxide layer 42 is used to form spacers during a subsequent etched-back step (Hong's Figs. 3E, 3F, 4E and 4F; col.5, lines 24-47). Such uses of the oxide layer are not relevant to Claims 1 and 7, which are designed to achieve high registration for subsequent photolithographical steps and to prevent charge leakage, as discussed above. Thus, the prior art references cited by the Examiner provide no motivation or suggestion for combining their teachings in the manner suggested by the Examiner. Accordingly, Applicants respectfully submit that Claims 3, 9 and 14-15 are each allowable over the cited prior art references, whether individually or in combination.

For the above reasons, Applicants respectfully request reconsideration of all pending claims (i.e., Claims 1-12 and 14-15) and allowance of these claims. If the Examiner has any question regarding the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants at 408-453-9200.

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on January 16, 2001.

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